

IEEE802.3bt
LLDP adhoc

Meeting #3: Rev 001, Tuesday June 27, 2017

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Meeting # 03 Attendees.

Name	Employed by:	Affiliated with:	Present:
Bruce Nordman	IBL	LBL	
Chad Jones	Cisco	Cisco	Y
Chris Bullock	Cisco	Cisco	
David Tremblay	HPE	HPE	Y
Geoff Thompson	Unemployed	Unaffiliated	Y
Heath Stewart	ADI/LT	ADI/LT	
John Skinner	Sifos	Sifos	Y
Yair Darshan	Microsemi	Microsemi	Y
David Law	HPE	HPE	Y
Murat Karaorman	ADI/LT	ADI/LT	Y
David Stover	ADI/LT	ADI/LT	Y
Lennart Yseboodt	Philips	Philips	Y



Proposed Agenda for meeting #01

- Starting at 18:00 IDT. Ending at 19:00 IDT.
Chad has volunteered to take notes of this meeting.

#	Time	Subject	Owner
1	18:00 – 18:05	<ul style="list-style-type: none">•Introduction•Patent policy•approving meeting minutes from last two meetings•Approving proposed Agenda for this meeting	Yair
2	18:05 – 18:10	Reviewing A.I. from last meeting.	Yair
3	18:10 – 18:20	Reviewing modified table for D2.5 concept with new proposals	Yair
4	18:20 – 18:23	Reviewing response to comment #297	Group
5	18:23 - 18:25	Reviewing response to comment #130	Group
5	18:25 – 19:35	Reviewing response to Lennart presentation from meeting #2	Group
6	19:35 – 19:50	<i>Reviewing proposed baseline sent by Yair</i>	<i>Group</i>
7	18:50 – 19:00	Summarizing of A.I. and points of agreements	Yair



Introduction and other businesses 09:00 – 09:05

- **The purpose** of this ad-hoc is to resolve LLDP state machine related comments from D2.4 and related issues for PSE and PDs prior sponsor ballot for D3.0.
- **Patent Policy**
 - Please read the Patent Policy slides at <http://www.ieee802.org/3/patent.html> prior the meeting.
 - Approving meeting minutes from last meeting
- **Meetings process.**
 - During the meeting: Questions only after presenter done with his presentation.
 - Follow the agenda as much as possible. Other issues can be tabled to be discuss later at the meeting, over the reflector, or at the next meeting agenda.
 - Discussions over the reflector prior the meeting is valuable and saves time during the meeting to reach consensus.
 - **After the meeting, please send your affiliation and attendance confirmation by email.**



Discussion and A.I From last meeting.

- Yair to generate Table with all the fields so we can address each field separately.
 - **DONE**
- Group to verify that they are OK with the proposed changes in the state machine per the response to comment #297.
- Group to verify that they are OK with the response to comment #130.
- Group to review and discuss over mail Lennart proposed changes.



LLDP concept review as agreed in D2.5 – Updated per the current text Proposal for a change marked in RED. Agreed concept marked in BLUE.

PD requested power value	PSE allocated power value	PD requested power value Mode A	PD requested power value Mode B	PSE allocated power value Alternative A	PSE allocated power value Alternative B
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#	PSE Type	Operating over	Connected to a PD	TLV field			
				pse_allocated_power	pd_requested_power	pse_allocated_power_Alt(X)	pd_req_power_mode(X)
				Y	Y	X (A or B or both)	X (A or B or both)
1	3/4	4-pairs	SS	1-999	1-999	0	0
2	3/4	2-pairs	SS	1-999	1-999	0	0
3	3/4	4-pairs	DS	1-999, Y=A+B (**) Lennart+Yair: Y=0.	1-999, Y=A+B (**) Lennart+Yair : Y=0.	1-499	1-499, Use A and B. Y=A+B.
4	3/4	2-pairs	DS	1-499, Y=A+B (**) Yair: Y=Alt(X) where X is the active pair instead of Y=A+B. Lennart: A and B=0. Yair: will not work. We need Y=Alt(X) per the simulations. PSE Y need to work with PD Y. If A=B=0 how will we know that Y is correct and is sync with A or B? David Tremblay : In the transition for 4-pair to 2-pair what should be the minimum value that goes to Y. Suggested is to go to the value of the last allocated value of A or B. (to be added to the description and not to the state machine)	1-499, Y=A+B (**) Yair+Lennart: Y=mode(X) where X is the active pair instead of Y=A+B.	1-499. Y=Alt (X), X is the active pairs. Yair: To add: (*) if Alt(X) is inactive, set to value 0.	1-499. Use A and B. (*) if mode(X) is inactive, set to value 0. Lennart+Yair: To resolve #297, delete (*). Y=mode(X), X is the active mode.
5	1/2	2-pairs	DS	1-499, May Y=A+B Similar to line 4 with the open question if Type 1 and 2 can use the new TLV fields.	1-499, Y=A+B (**) Similar to line 4.	1-499. Similar to line 4.	1-499. Use A and B. (*) if mode(X) is inactive, set to value 0. Similar to line 4.

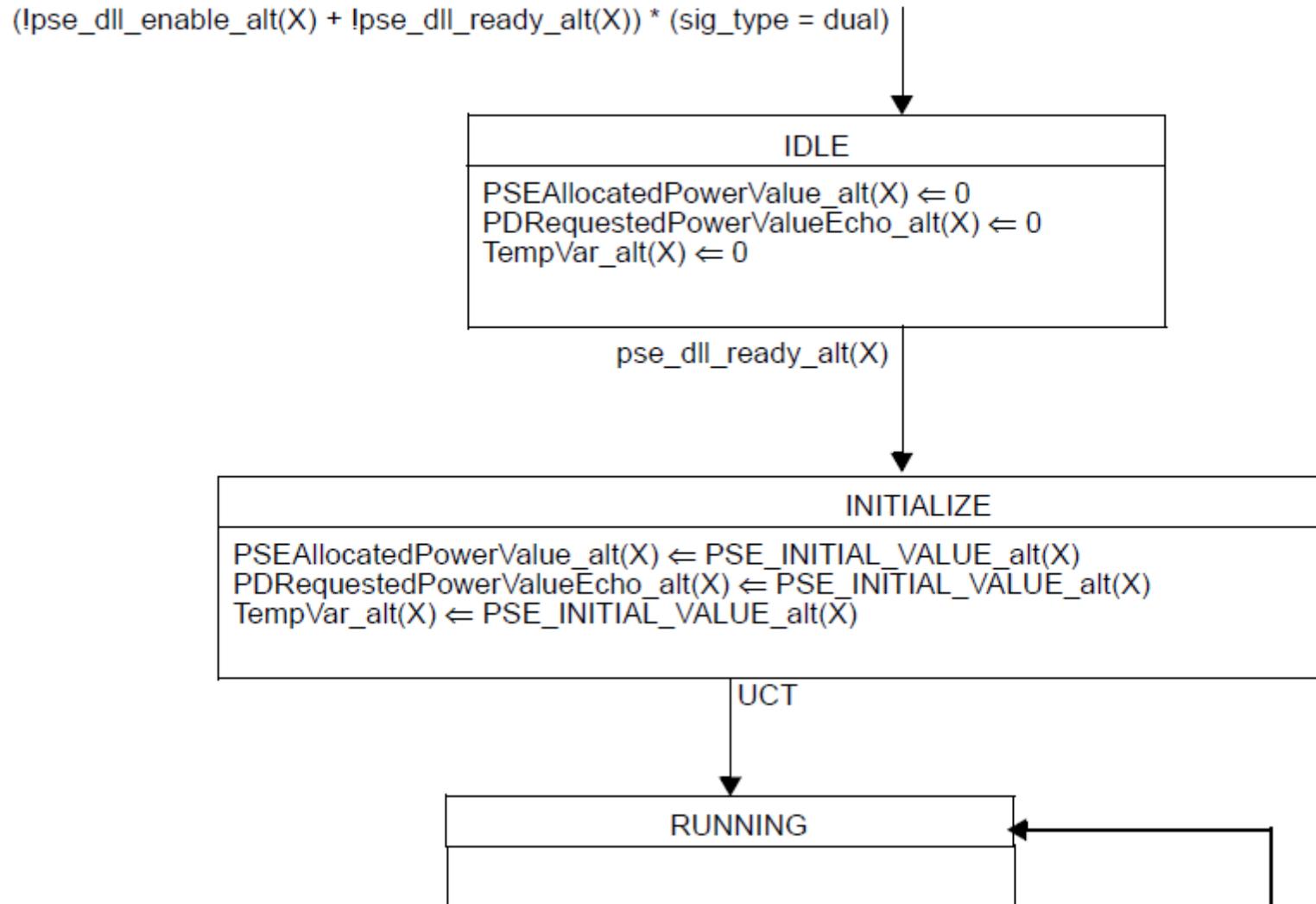
The above Table covers all use cases (Type 3/4 connected to Single-signature or dual-signature PD over 4-pairs or 2-pairs and switching between 4-pairs to 2-pairs and back to 4-pairs.

(*) See IDLE state in Figure 145-45 and Figure 145-46 for supporting this use case.

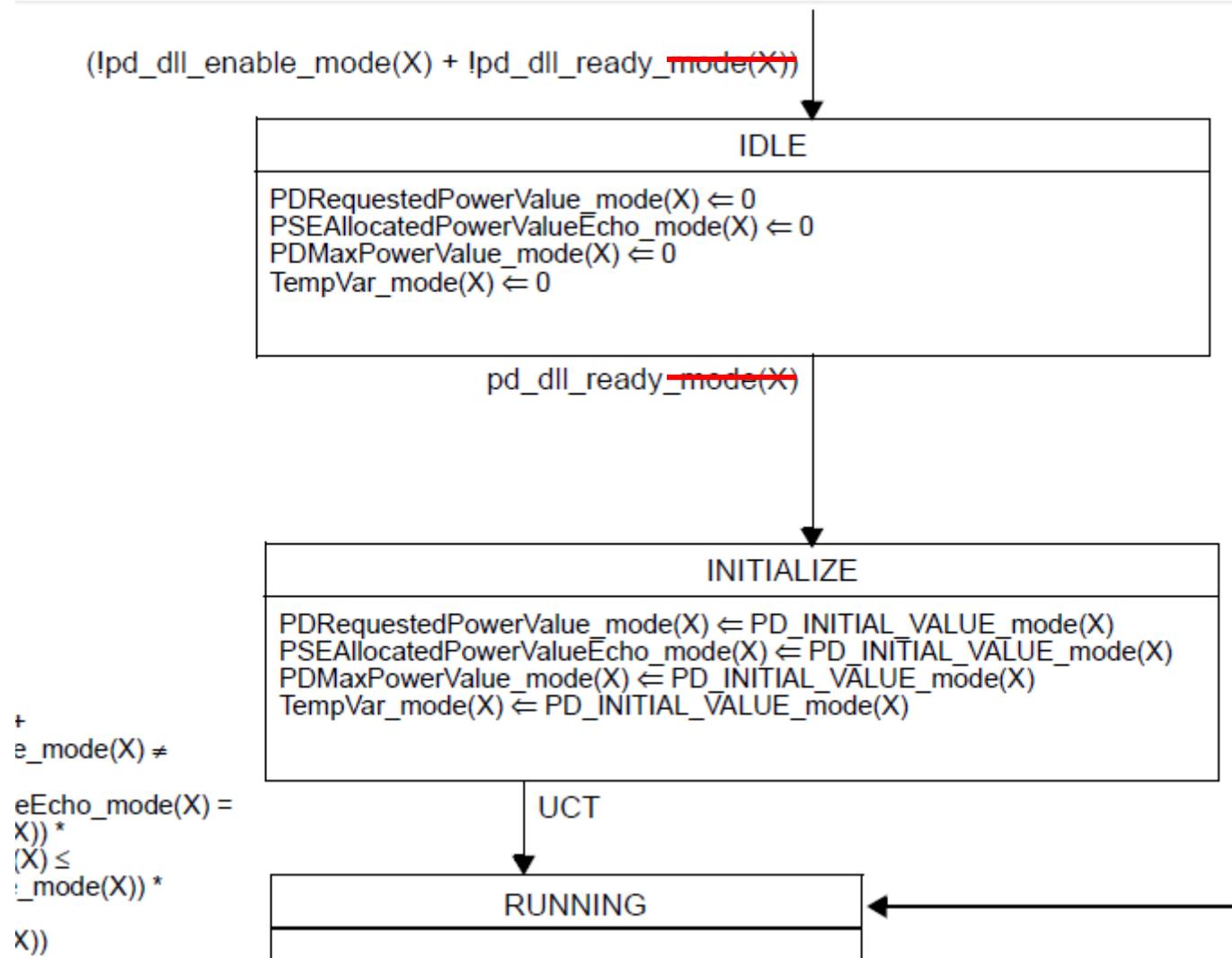
(**) See Annex A for why we need Y=A+B and the alternative solution for it (to use “PSE maximum available power” in 79.3.2.6e. This resolve argument #2 in Annex A)



Comment #297 D2.4 (Page 75 line 12 in D2.5) - Figure 145-43



Comment #297 D2.4 (Page 75 line 12 in D2.5) - Figure 145-44
 Proposal for a change marked in RED. Group is OK.



LLDP concept review as agreed in D2.5 – Updated per the current text Proposal for a change marked in RED.

- Discussion
 - The Table in previous slide is the current concept per D2.5. This closes questions from meeting #1 regarding item 4 and item 5 in the Table presented in meeting #1 (See Annex) regarding if it should be $Y=A+B$ or $Y=A$ or $Y=B$.

Yair+Lennart discussion:

- $Y=A+B$ can be replaced to $Y=\text{mode}(X)$ in the PD and $Y=\text{Alt}(X)$ in the PSE. This is alternative solution to argument #1 in Annex A and will resolve the double information of A, B and $Y=A+B$ confusion argument raised by Lennart.
- We have the information of total available power in the field “PSE maximum available power” in 79.3.2.6e. This resolve argument #2 in Annex A.
- To resolve #297, Lennart suggests: In order to request power on the unpowered pairset, see proposed changes in the red text. In addition, the `pd_dll_ready_mode(X)` need to be changed to `pd_dll_ready` to allow progressing to the INITIALIZE state in case PD want power on the unpowered pairset. No changes required in the PSE portion.
- Yair it will work:
- The proposal is:
 - To change from `pd_dll_ready_mode(X)` to `pd_dll_ready` in the PD state machine.
 - To change “if this mode/Alt is inactive, set to value 0” to “if this Alt is inactive, set to value 0” i.e. keep this requirement only to PSE.
- Group is OK.



Comment #297 D2.4 (Page 75 line 12 in D2.5)

- Comment #297 D2.4 (D2.5 Page 78 line 46)
"If Mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0."
 - What is this trying to do ? The PD may wish to ask for power on an unpowered Mode...

Suggested Remedy

Strike sentence.

- ACCEPT IN PRINCIPLE.

no changes to draft.

An LLDP ad hoc was formed

Yair: What we are trying to do is:

- In Figure 145-44 and Figure 145-45 power control state diagrams when connected to dual-signature PD, we add in D2.3 an IDLE state in order to resolve non active Alternative(X) or no active mode(X) by setting the relevant variables to zero prior going to INITIALIZE state.
 - Figure 145-45: PSEAllocatedPowerValue_alt(X), PDRequestedPowerValueEcho_alt(X) and TempVar_alt(X)
 - Figure 145-46: PDRequestedPowerValue_mode(X), PSEAllocatedPowerValueEcho_mode(X), PDMaxPowerValue_mode(X) and TempVar_mode(X)



Comment #297 D2.4 (Page 75 line 12 in D2.5)

Discussion:

Yair: See concept description for why we did it.

A.I: Group to verify that they are OK with the state machine in Figure 145-43 and Figure 145-44.

- Lennart response: The proposed response to this comment is to adopt:
 - To change from `pd_dll_ready_mode(X)` to `pd_dll_ready` in the PD state machine.
 - To change “if this mode/Alt is inactive, set to value 0” to “if this Alt is inactive, set to value 0” i.e. keep this requirement only to PSE.
- **Group to discuss.**
- **GROUP OPINION? Group is OK.**
 - The modifications proposed to the state machine in Figure 145-43?
 - To change from `pd_dll_ready_mode(X)` to `pd_dll_ready` in the PD state machine.
 - To change “if this mode/Alt is inactive, set to value 0” to “if this Alt is inactive, set to value 0” i.e. keep this requirement only to PSE.



Comment #130, #293 D2.4 (D2.5 Page 74 line 11)

Added text, "Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension."

Incorrectly blocks legacy types from using TLVs, Power status, System setup, PSE maximum available power, Autoclass, and Power done. The existing text does indicate what legacy Types are required to place in all Type 3 and Type 4 extension fields.

Suggested Remedy

Strike the called-out text.

ACCEPT IN PRINCIPLE.

OBE by 293

Comment 293 has the following response:

ACCEPT IN PRINCIPLE.

No changes to draft.

LLDP ad hoc was formed.

Discussion:

Yair: The proposed response to delete this text make sense. No reason to block new features from existing Type 1 and 2. Strike the called out text.

Geoff: All "shalls" should be in clause 145.

Heath: We agree to delete the text if PSE/ PD requested/allocated power mode A/B is set to zero when Type 1 and Type 2 PSE are used.

Jhon/Yair: In this case of Type 1/2 PSE connected to dual-signature PD, the fields are already defined. We need to focus only on the PSE fields since DS PD has access to all fields.

Lennart: @Heath, makes only sense to PSE allocated power. Doesn't make sense to PD requested power.

Yair: Not clear why @Heath makes sense only to PSE. If PSE can use the new fields for legacy PSEs, why not to use the same rules used in Type 3, 4 PSEs that have access to this field by default. The idea is to enable legacy PSEs to benefit from new features and not to disable them.

Heath A.I to generate comment and remedy for discussion for next time.

David Stover: It looks that we have covered this issue in this meeting adhoc presentation and/or by Lennart presentation.



Comment #130, #293 D2.4 (D2.5 Page 74 line 11) – Cont.

David Stover: I certainly understand the desire to extend support for e.g. power price index, parametric measurement reporting, etc. to Clause 33 (C33) devices that can support the extensions. However, if all of these TLV extensions are made available to C33 devices, I believe there is insufficient guidance in Clause 79 to enforce the desired limitations on a C33 device. For example, the TLV extensions allow PSEs to indicate they provide 4 pair power, to indicate and negotiate up to 99.9W of power, and to indicate they are a Type 3 or Type 4 PSE. Certainly, C33 PSEs should not be allowed to indicate this information to a PD. In particular, raising the power level for 2 pair systems is prohibited by our PAR. To resolve this comment we'll also need to come to agreement on the additional limitations placed on C33 devices when using the TLV extensions.

Lennart: The Clause 33 state diagrams already have a limit of 25.5W for DLL negotiation. So there is no problem in this case.

Lennart: The only reason I made the comment to get rid of that shall, is for the 4PID bit. Everything else is either "does not apply", or "pretty clear what to do".

Lennart: I'm not sure I see what limitations need to be defined that are not already clearly in Clause 33 ?

Yair: Comment #293 is similar and addressed in addition to 4PID bit the other new features we can use in Type 1 and 2 with the new TLV fields.

Yair: David: Can you make a list of TLVs that you believe need to be addressed with limitations.

GROUP OPINION? Do we agree to delete the proposed text?



New topic – do we need the $Y=A+B$ as currently in the spec?

- We agree that D2.5 is describe in the tables. And next meeting to present new table with the changes proposed – Group OK.
- Lennart presentation
- Yair inputs for the reasons we did it (See Annex A).
- Discussion
- Lennart: We have the information of total available power in the field “PSE maximum available power” in 79.3.2.6e. This resolve argument #2 in Annex A.
- Yair: Agree.
- Yair: Group is OK



Discussion and A.I for next meeting.

- Group to verify that they are OK with the response to comment #130.
- A.I: David Stover will make a list of the new TLVs that he believes need to be addressed with limitations when used by Type 1 and 2 PSEs.
- A.I: John Skinner to review line 4 in the table and the state machine.
- Group to review and discuss over mail Yair review to Lennart proposed concept changes. See http://www.ieee802.org/3/bt/public/lldpadhoc/DS_LLDP_Concept-with%20Yair%20comments_REV004.pdf
- Group to review proposed baseline: See http://www.ieee802.org/3/bt/public/lldpadhoc/Baseline%20for%20review%20-%20LLDP_adhoc.pdf



Points of agreements

- Meeting #2: Group agrees that the tables reflect the current spec in D2.5.
- Meeting #3: Group agrees to the concept changes in the Table **marked with BLUE text**.
- Meeting #3: Group agrees to the proposed changes to PD DLL state machine Figure 145-43.
- Meeting #3: Group agrees to the proposed response to comment #297 D2.4
- Meeting #3: Group agrees to use total available power in the field “PSE maximum available power” in 79.3.2.6e instead of $Y=A+B$ in the PSE for both single signature and dual signature. It will not be part of the state machine but it is available to the user as the rest of the new TLVs.



Annex A: Why we need $Y=A+B$ as currently in the spec?

Argument #1

- When we do LLDP simulations between Type 1, 2 PSE connected to dual-signature PD we encounter the following problem:
- Type 1, 2 PSE has only the `pse_allocated_power` field. He doesn't know about any other field such `pd_requested_power_modeA` or `B` fields/values.
- It means that PSE Type 1 and 2 can communicate with any PDs with `pse_allocated_power` and `pd_requested_power` fields only.

Now let's see what is going on step by step:

- PD puts values in `pd_requested_power_modeA` and `B` fields (what ever the values are)
- `pd_requested_power_modeA` and `B` fields are send through LLDP protocol and PSE tries to read it.
- PSE has only access to the content of `pd_request_power_value` because it doesn't know any other fields. If the content of `pd_request_power_value` in dual-signature PDs will be zero and not `pd_request_power_value = pd_request_power_value_modeA + pd_request_power_value_MODEb`, the PSE will see ZERO as the `pd_request_power_value` so the `pse_allocated` power value will be ZERO as well. So how it will work?
- The solution is: If in the PD we will set `pd_request_power_value = pd_request_power_value_modeA + pd_request_power_value_modeB` then `pse_allocated_power_value` can work with `pd_requested_power_value`. **Alternative solution for the 2-pair case: `pd_request_power_value = pd_request_power_value_mode(X)` where `X` is the active pairset.**



Annex A: Why we need $Y=A+B$ as currently in the spec? -2

Argument #2

- Imagine that you have a dual signature that want on modeA=45W and modeB=30W.
- But, PSE has only 29W.
- The question is how PSE will allocate the power. Please note the you have a single main power supply and the PSE **first** decides how to allocated power per port (i.e. the power needed per the whole port and then per the alternatives per the PD assigned class for each pair set (this is the only way it works in PSEs).

Now, Per the rules:

- PD mode A wants 45W but PSE has total 29W or <29W or whatever for mode A.
- PD mode B wants 30W but PSE has total 29W or <29W or whatever for mode B.
- So what PSE will do?
- Option 1: PSE will allocate power per the previous ratio (30W/45W). But this is not defined.
- Option 2: PSE will allocate power by splitting the 29W to half for each mode. But this is not defined
- OR option 3: PSE supply the total power as well (The sum field) and PD will decide what to do in order that the whole PD will work or one of the PD modes will work or nothing will work.

This is the best option. Why? Because this scenario is no different than the case when PSE is connected to single signature PD that wants 51W and PSE has only 30W. In this case, you give PD only 30W and let PD to decide how to use it. Please remember that in all dual signature PDs mode A and mode B are talking to each other by a single MCU.

Other alternative solution to this problem is to use the field “PSE max available power” which should be the total port power. We need to clarify in 79.3.2.6e that this value is applicable for PSE that supports single-signature and dual-signature.



Annex A: Why we need $Y=A+B$ as currently in the spec? -2

- Argument #3

High level power management care only for the total port power. The power management per pairset is kind of sublayer of the power management system. It is useful to pass the total power through the TLVs field. This is in general how current PSEs systems works.

Other alternative solution to this problem is to use the field “PSE max available power” which should be the total port power. We need to clarify in 79.3.2.6e that this value is applicable for PSE that supports single-signature and dual-signature.



Annexes

